<u>**CLAIMS**</u>

Please amend the claims as follows:

1.   (canceled)

2.   (previously presented)   In a data processing system having multiple processors each having a processor core, store queue (STQ) mechanism, read claim (RC) mechanism, and associated processor cache, a method for facilitating cache line updates responsive to processor-issued store operations, said method comprising:

determining when a store queue entry selected for dispatch by an RC machine provides an update to an entire cache line by:

tracking processor issued store operations gathered to said store queue entry via byte enable bits, wherein each storage granule of multiple storage granules within said store queue entry is provided a corresponding byte enable bit that is set to a logical high value when the storage granule is updated by a store operation, wherein the byte enable bit retains a logical low value when no update occurs to the corresponding storage granule, wherein each of multiple byte enable bits corresponding to the multiple storage granules are set to the logical high value when all the storage granules within the entry have been updated;

logically ANDing each of the multiple byte enable bits of the store queue entry to determine when all storage granules of said store queue entry have been updated; and

providing a full signal to a STQ controller when said logically ANDing step results in a logical high value, which indicates that all storage granules of said entry have been updated; and

completing said update to said entire cache line with address-only operations, wherein no data tenure is requested when an entire cache line is being overwritten, wherein said completing includes:

receiving at said RC mechanism an entry select identifying the entry for dispatch;

receiving at said RC mechanism a signal indicating that the entry is full;

assigning the cache line update operation to an RC machine of said RC mechanism;

providing an indication to the RC machine that the entire cache line is being updated; and

responsive to a receipt by said RC machine of the full signal indicating that the entry being dispatched is full, activating a cache update mechanism that enables the completion of the cache line update without requiring a copy of the cache line or current data within the cache line, wherein cache line updates from entries that are not full are completed with a current copy of the cache line within the cache and write permission to the cache line.

3.   (previously presented)   The method of Claim 2, wherein said store queue mechanism includes the STQ controller, said method further comprising:

tagging said entry as eligible for dispatch when said full signal is received at said STQ controller; and

enabling selection of said entry by arbitration logic of said STQ controller.

4.   (original) The method of Claim 3, further comprising:

notifying the RC mechanism when said entry has been selected for dispatch; and

signaling said RC mechanism when said entry is full.

5.   (original) The method of Claim 4, further comprising:

automatically resetting said byte enable bits for the entry when the entry is dispatched to an RC machine of said RC mechanism, wherein a full signal is reset to no longer indicate the entry is full.

6-7.   (canceled)

8.   (currently amended)   The method of Claim [[1]] 2, wherein following a miss at said processor cache or a hit at said processor cache with a cache line that becomes stale prior to completion of said update, said completing step comprises:

issuing an address-only operation to obtain write permission for said cache line; and

automatically updating said cache line with data from said entry once said write permission is obtained.

9-22.   (canceled)